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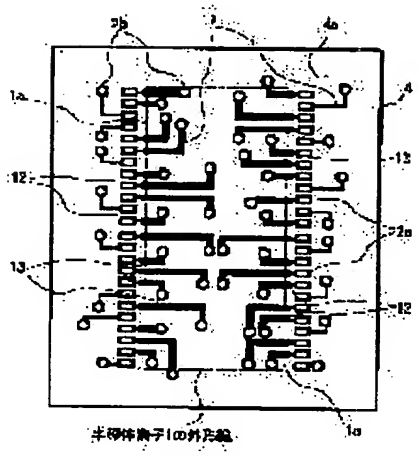
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent disconnection of a conductive wiring for improved reliability by, making a width at a position facing an outer edge of a semiconductor element to be wider than that at a position facing outside and/or inside of the outer edge of the semiconductor element.
SOLUTION: A conductive wiring comprises a surface wiring 2, a through hole, and an internal wiring, etc. A semiconductor element 1 is fixed to a semiconductor element fixing surface 4a of a printed wiring board 4, while jointed to a bonding pad 2a by a metal thin line. In surface wiring, a wide part 13 is provided at a surface wiring part 12 crossing just below a semiconductor element outer edge (end part) 1a so as to cross an profile line of the semiconductor element 1. Related to the wide part 13, wiring width between through holes is formed wider from the end part 1a. The deformation amount of an insulating film is minimum at the center of the semiconductor element 1 while maximum at the end 1a, and deformation of the insulating film is suppressed at the end 1a for suppressing cracks at the insulating film from occurring.



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[Claim(s)]

[Claim 1] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned substrate, and], In the semiconductor device formed so that it might have the semiconductor device arranged in the opposite side through the glue line and the aforementioned conductive wiring might connect to the aforementioned substrate of this insulator layer an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The aforementioned conductive wiring is a semiconductor device currently formed so that the rim section of the aforementioned semiconductor device and the width of face of the position which counters may become larger than the width of face of an outside [section / rim / of the aforementioned semiconductor device] and/or the inside, and the position that counters.

[Claim 2] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned substrate, and], In the semiconductor device formed so that it might have the serniconductor device arranged in the opposite side through the glue line and the aforementioned conductive wiring might connect to the aforementioned substrate of this insulator layer an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device Among the aforementioned conductive wiring, the rim section of the aforementioned semiconductor The conductive wiring formed in the center section of each side to constitute and the field which counters is a semiconductor device currently formed so that the rim section of the aforementioned semiconductor device and the width of face of the position which counters may become larger than the width of face of an outside [section / rim / of the aforementioned semiconductor device] and/or the inside, and the position that counters.

[Claim 3] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementi ned substrat , and], In th semiconductor device formed so that it might have the semiconductor device arranged in the opposite side through the glue line and the aforementioned conductive wiring might connect to the aforementioned

substrate of this insulator lay r an outsid [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The aforementioned conductive wiring accomplishes a group and is formed. The conductive wiring located in the ends of the conductive wiring which accomplished this group and was formed is a semiconductor device currently formed so that the rim section of the aforementioned semiconductor device and the width of face of the position which counters may become larger than the width of face of an outside [section / rim / of the aforementioned semiconductor device] and/or the inside, and the position that counters.

[Claim 4] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned substrate, and], In the semiconductor device formed so that it might have the semiconductor device arranged in the opposite side through the glue line and the aforementioned conductive wiring might connect to the aforementioned substrate of this insulator layer an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The aforementioned conductive wiring is a semiconductor device currently formed in fields other than the center section of each side which constitutes the rim section of the aforementioned semiconductor, and the field of the aforementioned substrate which counters.

[Claim 5] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned substrate, and], In the semiconductor device formed so that it might have the semiconductor device arranged in the opposite side through the glue line and the aforementioned conductive wiring might connect to the aforementioned substrate of this insulator layer an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The aforementioned conductive wiring is a semiconductor device currently formed so that the rim section of the aforementioned semiconductor device may be crossed aslant.

[Claim 6] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductiv / aforementioned / one principal plan of the af rem ntioned substrate, and], In th semiconductor d vic formed so that it might

hav the semiconductor device arrang d in the opposite sid through the glue line and the afor mentioned conductive wiring might connect to the af rementioned substrate of this insulator layer an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The semiconductor device constituted so that the relation between the elastic modulus E1 of the aforementioned insulator layer and the elastic modulus E2 of the aforementioned glue line in E1 <=E2 might become.

[Claim 7] The substrate which has one principal plane, and the conductive wiring formed in one principal plane of this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned substrate, and], In the semiconductor device formed so that it might have the semiconductor device arranged in the opposite side through the glue line and the aforementioned conductive wiring might connect to the aforementioned substrate of this insulator layer an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The semiconductor device whose elastic modulus of the aforementioned insulator layer is 10 or more Gpas.

[Claim 8] The aforementioned substrate is a semiconductor device given in the claim 1 which is an insulating tape, or any 1 term of 7.

[Claim 9] The insulating tape which has one principal plane, and the conductive wiring formed in one principal plane of this insulating tape, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned insulating tape, and], It has the semiconductor device arranged in the opposite side through the glue line with the aforementioned insulating tape of this insulator layer. The aforementioned conductive wiring is a semiconductor device which the aforementioned conductive wiring has exposed to the insulating aforementioned tape side of the edge of the aforementioned semiconductor device in the semiconductor device formed so that it might connect an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device.

[Claim 10] The insulating tape which has one principal plane, and the conductive wiring formed in one principal plane of this insulating tape, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned insulating tape, and], It has the semiconductor device arranged in th opposite side through the glue lin with the aforem ntioned insulating tape of this insulator layer. The aforementioned conductive wiring is a semiconductor device with

which the aforemention d insulator lay r is formed in the field which requir s the insulation with the aforementioned conductive wiring inside the rim section of the aforementioned semiconductor device in the semiconductor device formed so that it might connect an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device.

[Claim 11] The insulating tape which has one principal plane, and the conductive wiring formed in one principal plane of this insulating tape, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned insulating tape, and], It has the semiconductor device arranged in the opposite side through the glue line with the aforementioned insulating tape of this insulator layer. In the semiconductor device formed so that the aforementioned conductive wiring might connect an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device The semiconductor device with which the member which restrains deformation of the aforementioned insulator layer is formed in the field inside the rim section of the aforementioned semiconductor device of the aforementioned insulating tape, and the field which counters.

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the semiconductor device which was applied to the semiconductor device equipped with the conductive wiring which connects a semiconductor device and an external terminal electrically, especially raised the reliability of conductive wiring.

[0002]

[Description of the Prior Art] Since it corresponds to high-density-assembly-ization of a semiconductor device, the ball grid array (BGA) type semiconductor device suitable for the formation of many pins, a miniaturization, and improvement in the speed is put in practical use. The BGA type semiconductor device has structure which carried out two-dimensional arrangement of the shell external terminals, such as a solder bump, into the field of the package of a semiconductor device. In the BGA type semiconductor device, the member called interchange POZA by which conductive wiring is formed in a front face or a front face, and the interior is used for the electrical installation of a semiconductor device and an external terminal. The insulating tape which formed conductive wiring in the front face etc. at interchange POZA by making into a base material th printed-circuit board which makes glass/ poxy a base material, the polyimide used with the semiconductor device by

tape-automated-bonding (TAB) technology is used.

[0003] The example of the conv ntional semiconductor device which us d the printed-circuit board for interchange POZA is indicated by the U.S. patent NO. 5216278 and ****** No. 506319 [six to] official report etc. The example of the BGA type semiconductor device by these conventional technology is shown in drawing 30 and drawing 31 . In addition, the cross section of the BGA type semiconductor device of the former [drawing 30] and drawing 31 are the plans in the state where the semiconductor device, the conventional closure resin, and conventional insulator layer of a semiconductor device which were shown in drawing 30 were removed.

[0004] The printed-circuit board 4 which has the insulator layer 3 formed so that conductive wiring might be formed in a front face and the interior and the conventional BGA type semiconductor device might carry out opening of a part of conductive wiring to a semiconductor device 1, The metal thin line 6 which connects electrically the jointing material 5 which fixes a semiconductor device 1 on a printed-circuit board front face, and a semiconductor device 1 and conductive wiring of a printed-circuit board, It consists of the semiconductor device 1, a metal thin line 6, a closure resin 7 that closes semiconductor device root face 4a of a printed-circuit board 4, and an external terminal 8. Conductive wiring consists of front wiring 2, bonding pad 2a, through hole 2b, internal wiring 2c, and land 2d. The insulator layer 3 is called the solder resist or photoresist, and is formed by screen printing, the photograph method, etc. Material, such as epoxy, a polyimide, and a polybutadiene, is used for an insulator layer.

[0005] The metal thin line 6 and conductive wiring of a printed-circuit board 4 are connected by bonding pad 2a arranged outside the field of a semiconductor device 1. In a bonding pad 2a portion, opening 3a is formed in the insulator layer 3, and bonding pad 2a can be joined now to the metal thin line 6. The external terminal 8 is formed in external terminal plane-of-composition 4b of a printed-circuit board in the shape of a grid, and is arranged at both outside the field of a semiconductor device 1, and within a field. In order to connect electrically the external terminal 8 and semiconductor device 1 which are arranged in the 1st page of a semiconductor device, front wiring 2 is formed to land 2d which is continuously formed so that the visible outline of a semiconductor device 1 may be intersected toward the inside of the field of a semiconductor device 1 from bonding pad 2a, and was formed in external terminal plane-of-composition 4b of the printed-circuit board to which the external terminal 8 is joined through through hole 2b or internal wiring 2c which stands in a row in front wiring. Op ning 9a is formed in the insulator layer 9 prepared

in external terminal plan -of-c mpositi n 4b of a printed-circuit board, and the land 2d section can join now land 2d and the external terminal 8.

[0006]

[Problem(s) to be Solved by the Invention] In the conventional semiconductor device, the coefficient of linear expansion of a semiconductor device 1 is [the coefficient of linear expansion of 2 - 3x10-6/degree C and a printed-circuit board] about 16x10-6/degree C, and the big difference to both coefficient of linear expansion is **. If a temperature change joins the semiconductor device of such composition, the thermal stress resulting from both coefficient-of-linear-expansion difference will come to occur in both interface, and a crack, breakaway, etc. will occur in the jointing material 5. If a crack etc. occurs in the jointing material 5, it will concentrate on edge 1a of a semiconductor device 1, and the thermal stress generated in both interface will become still larger. If a temperature change is repeatedly added in such a situation, as shown in drawing 32 (cross section showing the state of the crack of the insulator layer of the conventional BGA type semiconductor device), the edge 1a portion of a semiconductor device will be left insulator layer 3, and hiatus 11 will come to occur.

[0007] Next, it goes away insulator layer 3 and generating of hiatus 11 and the mechanism of growth are explained. Although both whole interface shares the thermal stress generated according to the coefficient-of-linear-expansion difference of a semiconductor device 1 and a printed-circuit board 4, if a crack 10 occurs in the jointing material 5, since it becomes impossible for the portion of this crack 10 to pay stress, stress will come to concentrate it on edge 1a of a semiconductor device. A crack 11 occurs in an insulator layer 3 by this stress concentration. Since the crack has arisen in that the coefficient of linear expansion of an insulator layer 3 is comparatively large, and the jointing material 5, an insulator layer 3 can deform freely by the temperature change. In connection with the repeat of a temperature change, it goes away insulator layer 3, and hiatus 11 advance gradually, repeating opening and embarrassment, and any come to grow up to be the crack which crossed the insulator layer 3.

[0008] If it is formed succeeding the inside (henceforth an inside) and the outside (henceforth superficies) of the rim section of a semiconductor device 1 so that front wiring 2 may go away above-mentioned insulator layer 3 and may cross semiconductor device edge 1a which is the generating part of hiatus 11, a crack 11 will advance also to th front wiring 2 int rior, and possibility that an open circuit will generat any in front wiring 2 will become large. A semiconductor device stops

functioning as front wiring being disconnected normally, and th reliability of a s miconductor device is made to fall remarkably.

[0009] The same problem is generated also in the semiconductor device which used the insulating tape used with the TAB technology in which conductive wiring was formed in the front face as interchange POZA.

[0010] this invention prevents and suppresses an open circuit of the conductive wiring currently formed succeeding the inside of the field of a semiconductor device, and the outside of a field so that the rim section (henceforth a visible outline) of a semiconductor device may be intersected, and it aims at offering a reliable semiconductor device.

[0011]

[Means for Solving the Problem] The above-mentioned technical problem is solvable by adopting a means to reduce or restrain big deformation of the insulator layer at the time of a temperature change being added produced when the crack etc. occurred in jointing material.

[0012] The conductive wiring with which this invention was formed in one principal plane of the substrate which has one principal plane, and this substrate, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned substrate, and], With the aforementioned substrate of this insulator layer, it is characterized by having had the semiconductor device arranged in the opposite side through the glue line, and having the following composition in the semiconductor device formed so that the aforementioned conductive wiring might connect an outside [section / rim / of the aforementioned semiconductor device], and inside the rim section of the aforementioned semiconductor device.

[0013] (A) The aforementioned conductive wiring should be formed so that the rim section of the aforementioned semiconductor device and the width of face of the position which counters become larger than the width of face of an outside [section / rim / of the aforementioned semiconductor device] and/or the inside, and the position that counters.

[0014] (B) The conductive wiring formed in the center section of each side which constitutes the rim section of the aforementioned semiconductor among the aforementioned conductive wiring, and the field which counters should be formed so that the rim section of the aforementioned semiconductor device and the width of face of the position which counters become larger than the width of face of an outside [section / rim / of the afor mentioned semiconductor d vic] and/or the inside, and

the position that counters.

[0015] In the target semiconductor d vice [this invention], it will b cover d with the insulator layer except for a part of openings by the conductive wiring on the front face of a substrate. Conductive wiring is formed of the material which galvanized on the front face of copper (Cu) or copper. From the material of an insulator layer, since the elastic modulus is usually large, deformation of the insulator layer at the time of a temperature change is restrained for the material used for conductive wiring by conductive wiring. Therefore, the deformation of an insulator layer can be reduced by making [many] the rate for which makes large wiring width of face of conductive wiring, and conductive wiring within an insulator layer accounts.

[0016] Drawing 33 is the result of analyzing the stress of the conductive wiring front face at the time of having taken out 1/4 portion of a BGA type semiconductor device, being the model in which-one conductive wiring was formed in the semiconductor device side, introducing a crack into the circumference of conductive wiring, and cooling a semiconductor device, and the relation of wiring width of face with a finite element method. the stress reduction effect by the increase in wiring width of face is clearer than drawing 33 , and, especially therefore, the thing for which wiring width of face of two or more conductive wiring is made large and for which stress reduction is aimed at further becomes possible in an actual semiconductor device

[0017] Moreover, in a part for the direct lower part of the semiconductor device edge (rim section) which an open circuit of conductive wiring generates, by making large wiring width of face of conductive wiring, even if a crack occurs in the conductive wiring other than the stress reduction effect by deformation reduction of an insulator layer, the effect which can lengthen a life (number of times of a repeat of a temperature change) until it results in an open circuit is also acquired.

[0018] With the semiconductor device which carried the rectangular semiconductor device, the amount of [which constitutes the visible outline of a semiconductor device] center section of four sides will be in plane strain condition, and since the thermal stress to generate becomes large, the probability which conductive wiring disconnects in this portion becomes high further again. Moreover, if wiring width of face is made larger than required, the wiring capacity within a semiconductor device will increase and a noise will occur, and it becomes the factor from which the high-speed operation of a semiconductor device is prevented. Therefore, by making large wiring width of face of the conductive wiring formed by part for the center s ction of th side of a s miconductor device wher the open-circuit probability of occurrence becomes large at least so that the visible outline of a semiconductor

device might b intersected, an open circuit can b prev nted and the s miconductor device also in c nsideration of the property of a semiconductor d vice can b obtained.

[0019] (C) The conductive wiring located in the ends of the conductive wiring which the aforementioned conductive wiring accomplished the group and was formed, and accomplished this group and was formed should be formed so that the rim section of the aforementioned semiconductor device and the width of face of the position which counters become larger than the width of face of an outside [section / rim / of the aforementioned semiconductor device] and/or the inside, and the position that counters.

[0020] Also by this invention, the conductive wiring with a big elastic modulus can enlarge the rate which occupies a printed-circuit board front face to an insulator layer, and can restrain deformation of an insulator layer. Moreover, there may be many terminals of a semiconductor device and it may be difficult to make large wiring width of face of all conductive wiring by the conductive wiring group which conductive wiring approaches and is arranged at abbreviation parallel. Moreover, when a BGA type semiconductor device carries the semiconductor device as which high-speed operation is required in many cases and makes conductive wiring width of face larger than required, wiring capacity (inductance) increases and high-speed operation may be checked by this. Therefore, it is necessary for expanding wiring width of face to minimize. By the aforementioned conductive wiring group, by making larger than internal wiring conductive wiring located in the edge at least, pinning of the deformation of an insulator layer can be carried out at both ends, and the deformation of an insulator layer can be reduced.

[0021] (D) The aforementioned conductive wiring should be formed in fields other than the center section of each side which constitutes the rim section of the aforementioned semiconductor, and the field of the aforementioned substrate which counters.

[0022] In the semiconductor device which carried the rectangular semiconductor device, since the amount of [of the side which constitutes the visible outline of a semiconductor device] center section will be in plane strain condition and the thermal stress to generate becomes large, the probability which conductive wiring disconnects in this portion becomes high. Therefore, possibility of open-circuit generating can be made small by forming a conductive circuit pattern so that conductive wiring which intersects th visible outline of a s miconductor device at a part for the above-mentioned center section, and crosses an edge may not be

arranged.

[0023] (E) The aforem ntioned conductive wiring should be formed to cross the rim section of the aforementioned semiconductor device aslant.

[0024] The rate to which the conductive wiring 2 occupies conductive wiring in the field of a semiconductor device by forming so that the visible outline of a semiconductor device may be crossed aslant can be enlarged, and the deformation restricted effect of an insulator layer becomes large. Moreover, the effect that a life since the cross section of the conductive wiring on the visible outline of a semiconductor device increases seemingly, after a crack occurs in wiring until it disconnects is prolonged can also be acquired.

[0025] (F) It constituted so that the relation between the elastic modulus E1 of the aforementioned insulator layer and the elastic modulus E2 of the aforementioned glue line in E1 <=E2 might become.

[0026] It generates and the crack of an insulator layer grows, when the insulator layer with a big coefficient of linear expansion itself repeats contraction and expansion by the temperature change. The material used for an insulator layer is an epoxy resin, polyimide resin, or a polybutadiene resin, and the elastic modulus of such material is usually larger than the elastic modulus of jointing material. Since the stress generated at the nose of cam of hiatus is not eased when the elastic modulus of an insulator layer is large, growth of a crack is accelerated as a crack becomes long. If the elastic modulus of an insulator layer is made small, the deformation in the nose of cam of a crack becomes easy, the stress at the nose of cam of a crack is eased, and growth of a crack can be inhibited.

[0027] Drawing 34 is the result of having taken out 1/4 portion of a BGA type semiconductor device, being the model in which-one conductive wiring was formed in the semiconductor device side, having introduced the crack into the circumference of conductive wiring, going away, when a semiconductor device is cooled, and analyzing the relation between the stress of the conductive wiring front face at the nose of cam of hiatus, and the elastic modulus of an insulator layer with a finite element method. When making the elastic modulus of an insulator layer small from drawing, it is proved that the stress at the nose of cam of hiatus is also reduced.

[0028] (G) The elastic modulus of the aforementioned insulator layer should be 10 or more Gpas.

[0029] When a crack and breakaway occurred in jointing material, deformation of an insulator layer gen rates fr ely th crack of the insulator layer constituting the cause of open-circuit g nerating of conductiv wiring in a bird clapper. Since it becomes

impossible to restrain d formation of an insulator layer wh n th elastic modulus of jointing material is small similarly, it becomes easy to generate a crack in an insulator layer. Therefore, if deformation of the insulator layer at the time of a temperature change is restrained by enlarging the elastic modulus of jointing material, it will become possible to inhibit crack generating of an insulator layer.

[0030] Drawing 35 is the model which took out the cross section of a BGA type semiconductor device, and is the result of changing the elastic modulus of jointing material and analyzing the insulator layer surface stress in the semiconductor device edge at the time of cooling a semiconductor device with a finite element method. The elastic modulus of an insulator layer is set to 2.5GPa(s) in this analysis. Although it is distinct that the stress of an insulator layer declines gradually if the elastic modulus of jointing material is enlarged from drawing, the fall rate of about 10 GPas to stress is small, and serves as a value of simultaneously regularity. If the elastic modulus of jointing material is set as 10 or more GPas from this result, the stress of an insulator layer is maintainable to a low value.

[0031] Moreover, by trial production evaluation which artificers performed, the crack generated the elastic modulus of jointing material in 100 repeats of a temperature change in the semiconductor device set to 1GPa at the insulator layer. However, in what set the elastic modulus to 17GPa(s), at least 400 times, it did not generate but the crack of an insulator layer was able to check the effect.

[0032] In addition, if the elastic modulus of jointing material is enlarged, the stress generated in a semiconductor device according to the coefficient-of-linear-expansion difference of a semiconductor device and a printed-circuit board will also become large, and possibility that a crack will occur in a semiconductor device will increase. Therefore, the range of the elastic modulus used for jointing material makes 10GPa(s) a minimum, and the value which does not make a semiconductor device generate a crack serves as an upper limit.

[0033] Moreover, the conductive wiring with which the semiconductor device of this invention was formed in one principal plane of the insulating tape which has one principal plane, and this insulating tape, The insulator layer formed in the desired field [wiring / conductive / aforementioned / one principal plane of the aforementioned insulating tape, and], It has the semiconductor device arranged in the opposite side through the glue line with the aforementioned insulating tape of this insulator layer. The aforementioned conductive wiring is characterized by having the following composition in the semiconductor d vice formed so that it might connect an outside [section / rim / of the aforementioned semiconductor d vice], and inside

the rim section of th aforementioned s mic nductor device.

[0034] (H) The afor mentioned conductive wiring be exposed to th insulating aforementioned tape side of the edge of the aforementioned semiconductor device.

[0035] That is, generating and growth of a crack can be suppressed by removing the insulator layer which a crack tends to generate from a part for the direct lower part of the semiconductor device edge which thermal stress concentrates, and covering this portion by the big closure resin of toughness from an insulator layer.

[0036] (I) The aforementioned insulator layer should be formed in the field which requires the insulation with the aforementioned conductive wiring inside the rim section of the aforementioned semiconductor device.

[0037] the conductor of others [insulator layer / wiring / conductive] -- it is prepared in order to protect so that a member etc. may be contacted and a short circuit etc. may not be caused Therefore, the deformation of the insulator layer at the time of a temperature change can be reduced by reducing the volume of the insulator layer in a semiconductor device side, as only the circumference of the conductive wiring by the insulator layer is covered.

[0038] (J) The member which restrains deformation of the aforementioned insulator layer should be formed in the field inside the rim section of the aforementioned semiconductor device of the aforementioned insulating tape, and the field which counters.

[0039] As for the member for a deformation restraint, forming by the foil-like member is desirable, and it is good to form with the same material as a conductive material. Moreover, in the semiconductor device which carried the rectangular semiconductor device, since the amount of [of the side which constitutes the visible outline of a semiconductor device] center section will be in plane strain condition and the thermal stress to generate becomes large, the probability which conductive wiring disconnects in this portion becomes high. Therefore, what is necessary is just to restrain deformation of the insulator layer for the center section of the side of a semiconductor device at worst.

[0040] Moreover, it is also effective in the elastic modulus of a front insulator layer equivalent to the elastic modulus of the aforementioned jointing material or to consider as less than [it].

[0041] It generates and the crack of an insulator layer grows, when the insulator layer with a large coefficient of linear expansion itself repeats contraction and expansion by the temperature change. The material used for an insulator layer is an epoxy resin, polyimide r sin, or a polybutadiene resin, and the elastic modulus of such material is

usually larger than the elastic modulus of jointing material. Since the stress generated at the nos of cam of hiatus is not ased when the elastic modulus of an insulator layer is large, growth of a crack is accelerated as a crack becomes long. If the elastic modulus of an insulator layer is made small, since the plastic deformation field in the nose of cam of a crack is expanded, the stress at the nose of cam of a crack is eased, and growth of a crack can be inhibited.

[0042]

[Embodiments of the Invention] Hereafter, it explains to the **** detail for examples which showed the drawing to the operation gestalt of this invention.

The [1st example] Drawing 1 is a plan in the state where the semiconductor device, closure resin, and insulator layer of a semiconductor device by the 1st example of this invention were removed, and drawing 2 is the cross section of the semiconductor device shown in drawing 1 .

[0043] In drawing, conductive wiring is formed in the front face and the interior of a printed-circuit board 4, and conductive wiring consists of front wiring 2, bonding pad 2a, through hole 2b, internal wiring 2c, and land 2d. The insulator layers 3 and 9 in which Openings 3a and 9a were formed are formed in the front faces 4a and 4b of a printed-circuit board 4. The rectangular semiconductor device 1 has fixed by the jointing material 5 to semiconductor device root face 4a of a printed-circuit board. A semiconductor device 1 and conductive wiring are electrically connected by the metal thin line 6, and the metal thin line 6 is joined to bonding pad 2a prepared outside the field of a semiconductor device 1. In a bonding pad 2a portion, opening 3a is prepared in the insulator layer 3, and the metal thin line 6 can be joined now. Conductive wiring is prolonged from bonding pad 2a through through hole 2b of the front wiring 2 on the front face of a printed-circuit board, and the printed-circuit board 4 interior, or internal wiring 2c to land 2d of external terminal plane-of-composition 4b of a printed-circuit board. When the external terminal 8 is joined by land 2d, a semiconductor device and an external terminal are electrically connected by conductive wiring. In a land 2d portion, opening 9a is prepared in the insulator layer 9, and the external terminal 8 can join now to land 2d. Semiconductor device root face 4a of a semiconductor device 1, the metal thin line 6, and a printed-circuit board is covered with the closure resin 7.

[0044] The broad section 13 is formed in the front wiring 12 which crosses the direct lower part of semiconductor device edge 1a so that the visible outline of a semiconductor device 1 may be intersected among the front wiring 2 formed in semiconductor device root face 4a of a print d-circuit board. The broad section 13 of

th front wiring shown in drawing 1 is formed by making large wiring width of face between through hole 2b from a semiconductor d vice edge 1a portion.

[0045] A copper (Cu) foil or the copper foil which plated gold (Au), nickel (nickel), etc. on the front face is used at front wiring 2. A printed-circuit board 4 consists of material which makes glass/epoxy a base material. Material, such as gold (Au), silver (Ag), or aluminum (aluminum), is used for the metal thin line 6. The epoxy resin filled up for example, with the silica particle is used for the closure resin 7. In case a semiconductor device is mounted, the solder (for example, Pb-Sn system eutectic solder) used widely is used for the external terminal 8.

[0046] According to the semiconductor device of this example, deformation of the insulator layer at the time of a temperature change being added can be restrained by the front wiring which prepared the broad section, and generating and growth of the crack of an insulator layer can be inhibited.

[0047] The example shown in drawing 1 showed the example which forms the broad section 13 in the front wiring 2 between [a part for the direct lower part of semiconductor device edge 1a to] through hole 2b. Since the deformation of an insulator layer 3 serves as the minimum at the center of a semiconductor device 1, and serves as the maximum at the end and maximum stress occurs in the direct lower part of edge 1a, it goes away insulator layer 3 and hiatus are generated in a semiconductor device edge 1a portion. For this reason, an indispensable effect will be acquired if deformation of an insulator layer is restrained in a semiconductor device edge 1a portion. Therefore, the broad section 13 should just be formed in a part for the direct lower part of semiconductor device edge 1a at least like drawing 3 . In the case of the semiconductor device which cannot enlarge wiring capacity, an example like drawing 3 becomes effective from the demand of high-speed operation especially.

[0048] The [2nd example] Drawing 4 is a plan in the state where the semiconductor device, closure resin, and insulator layer of a semiconductor device by the 2nd example of this invention were removed, and drawing 5 is the cross section of the semiconductor device shown in drawing 4 .

[0049] Since the basic composition as a semiconductor device is common in the 1st example, it omits explanation. In this example, it is formed in semiconductor device root face 4a of a printed-circuit board among front wiring 2, and as the visible outline of a semiconductor device 1 is intersected, it is the front wiring 12 which crosses the direct lower part of semiconductor device edge 1a, and th broad s ction 13 is formed in front wiring 12a arranged at cent r-s cti n part 1b of a semiconductor

d vice long side. The broad section 13 of th front wiring 12 shown in drawing 4 is formed by making large wiring width of face b tween through hole 2b from a part for the direct lower part of semiconductor device edge 1a.

[0050] In the semiconductor device which carried the rectangular semiconductor device 1 like this example, center-section part 1b of a semiconductor device long side will be in plane strain condition, for example, and the stress generated in the direct lower part of semiconductor device edge 1a of center-section part 1b becomes larger than the stress generated in semiconductor device corner section 1c. Therefore, since an open circuit of front wiring has the large probability generated in edge 1a of center-section part 1b by the side of a semiconductor device long side, an open circuit of front wiring can be prevented by making front wiring 2 of this portion broad, and restraining deformation of an insulator layer 3.

[0051] this example shows the example for which front wiring crosses the long side side edge section of a semiconductor device. However, in a semiconductor device which is arranged so that conductive wiring may cross the shorter side side edge section of a semiconductor device, you may form the broad section 13 also in the front wiring by the side of a shorter side.

[0052] The example shown in drawing 4 showed the example which forms the broad section 13 in the front wiring 2 between [a part for the direct lower part of semiconductor device edge 1a to] through hole 2b. Since the deformation of an insulator layer 3 serves as the minimum at the center of a semiconductor device 1, and serves as the maximum at the end and maximum stress occurs in the direct lower part of edge 1a, it goes away insulator layer 3 and hiatus are generated in a semiconductor device edge 1a portion. For this reason, an indispensable effect will be acquired if deformation of an insulator layer is restrained in a semiconductor device edge 1a portion. Therefore, the broad section 13 should just be formed in a part for the direct lower part of semiconductor device edge 1a at least like drawing 6 . In the case of the semiconductor device which cannot enlarge wiring capacity, an example like drawing 6 becomes effective from the demand of high-speed operation especially.

[0053] The [3rd example] Drawing 7 is a plan in the state where the semiconductor device, closure resin, and insulator layer of a semiconductor device by the 3rd example of this invention were removed, and drawing 8 is the cross section of the semiconductor device shown in drawing 7 .

[0054] Since the basic composition as a semiconductor device is common in the 1st example, it omits explanation. In this example, by the front wiring group 14 which

crosses dge 1a, the broad section 13 is formed in th front wiring locat d in edg 14a of a front wiring group so that two or more front wiring may intersect abbreviation parallel with the visible outline of a semiconductor device 1 among the front wiring 2 currently formed in semiconductor device root face 4a of a printed-circuit board, and wiring width of face is large from the front wiring located in internal 14b of a front wiring group. The broad section 13 of the conductive wiring shown in drawing 7 is formed by making large wiring width of face between through hole 2b from a semiconductor device edge 1a portion.

[0055] According to the semiconductor device shown in this example, by forming the broad section in the front wiring of the aforementioned front wiring group located in an edge at least, pinning can be carried out and generating and growth of the crack of an insulator layer can be inhibited by the front wiring which prepared the broad section of both ends for deformation of the insulator layer at the time of a temperature change being added. Moreover, since the example of drawing 7 can make the increase in wiring capacity the minimum, it becomes effective with the semiconductor device with which high-speed operation is demanded.

[0056] The example shown in drawing 7 showed the example which forms the broad section 13 among through hole 2b from a part for the semiconductor device edge 1a direct lower part of the front wiring 2 located in edge 14a of the front wiring group 14. Since the deformation of an insulator layer 3 serves as the maximum at the edge of a semiconductor device 1, it goes away insulator layer 3 and comes to generate hiatus in a part for the direct lower part of semiconductor device edge 1a. For this reason, an indispensable effect will be acquired if deformation of an insulator layer is restrained in a semiconductor device edge 1a portion. Therefore, the broad section 13 should just be formed in a part for the direct lower part of semiconductor device edge 1a at least like drawing 9 . In the case of the semiconductor device which cannot enlarge wiring capacity, an example like drawing 9 becomes effective from the demand of high-speed operation especially.

[0057] The [4th example] Drawing 10 is a plan in the state where the semiconductor device, closure resin, and insulator layer of a semiconductor device by the 4th example of this invention were removed, and drawing 11 is the cross section of the semiconductor device shown in drawing 10 .

[0058] Since the basic composition as a semiconductor device is common in the 1st example, it omits explanation. At this example, the front wiring 2 which crosses edge 1a so that th visibl outline of a semiconductor device 1 may be intersected is not f rmed in s miconductor device root fac 4a of a printed-circuit board by long side

side center-section part 1b of a semiconductor device. The front wiring 2 of this portion is prolonged toward the way outside th printed-circuit board 4 from bonding pad 2a, and is connected to land 2d through through hole 2b and internal wiring 2c. Therefore, in a part for the direct lower part of semiconductor device edge 1a of center-section part 1b, only an insulator layer 3 and the jointing material 5 are formed in semiconductor device root face 4a of a printed-circuit board. On the other hand, in the near portion of corner 1c of a semiconductor device, front wiring 2 is formed so that semiconductor device edge 1a may be crossed.

[0059] In the semiconductor device which carried the rectangular semiconductor device 1 like this example, center-section part 1b by the side of a semiconductor device long side will be in plane strain condition, for example, and the stress generated in a part for the semiconductor device edge 1a direct lower part of center-section part 1b becomes larger than the stress generated in semiconductor device corner section 1c. For this reason, the probability of generating an open circuit of conductive wiring in a part for the edge 1a direct lower part of center-section part 1b by the side of a semiconductor device long side becomes large. Therefore, in center-section part 1b by the side of a semiconductor device long side, an open circuit of the conductive wiring which goes away insulator layer 3 and originates in hiatus can be prevented by taking about so that front wiring 2 may not cross semiconductor device edge 1a.

[0060] The [5th example] Drawing 12 is a plan in the state where the semiconductor device, closure resin, and insulator layer of a semiconductor device by the 5th example of this invention were removed, and drawing 13 is the cross section of the semiconductor device shown in drawing 12 .

[0061] Since the basic composition as a semiconductor device is common in the 1st example, it omits explanation. In this example, it is the front wiring 2 formed in semiconductor device root face 4a of a printed-circuit board, and the front wiring 12 arranged at center-section part 1b by the side of a semiconductor device long side among the front wiring 12 formed so that the visible outline of a semiconductor device 1 may be intersected and semiconductor device edge 1a may be crossed is formed so that semiconductor device edge 1a may be aslant crossed to the visible outline of a semiconductor device 1.

[0062] The rate in which the front wiring 2 in the field of a semiconductor device 1 occupies front wiring 12 rather than the case where it crosses right-angled by forming so that edge 1a of a semiconductor device may be crossed aslant can be enlarged, and the deformation restricted effect of an insulator layer becomes large.

Moreover, th effect that a life since the cross section of th front wiring on a semiconductor device visible utline increases seemingly, after a crack occurs in wiring until it disconnects is prolonged can also be acquired.

[0063] In the semiconductor device which carried the rectangular semiconductor device 1 like this example, center-section part 1b by the side of a semiconductor device long side will be in plane strain condition, for example, and the stress generated in a part for the direct lower part of semiconductor device edge 1a of this portion becomes large. For this reason, the probability of generating an open circuit of conductive wiring in center-section part 1b by the side of a semiconductor device long side is large. Therefore, it is necessary to restrain deformation of the insulator layer 3 in center-section part 1b at least, and to reduce deformation.

[0064] The [6th example] Drawing 14 is the cross section of the semiconductor device by the 6th example of this invention.

[0065] Since the basic composition as a semiconductor device is common in the 1st example, it omits explanation. With the semiconductor device of this example, equivalent [in an insulator layer 3 / to the elastic modulus of the jointing material 5] or it forms with the material which has an elastic modulus not more than it. Since deformation of the insulator layer itself becomes easy even when a crack occurs in an insulator layer 3 by forming an insulator layer 3 into low elasticity, the stress generated at the nose of cam of a crack can be eased by deformation. Therefore, the effect which suppresses growth of the crack by the repeat of a temperature change can be acquired, and an open circuit of front wiring can be prevented.

[0066] The material whose elastic modulus is usually about 1 GPa is used for the jointing material 5. Therefore, it is desirable for an elastic modulus to choose and use the material of 1 or less GPa for an insulator layer 3.

[0067] Although it goes away insulator layer 3 and hiatus generating and growth can be inhibited by low elasticity-ization of an insulator layer 3 as described above, the elastic modulus of an insulator layer 3 may not be able to be made low from the restrictions on manufacture of a printed-circuit board 4 etc. In such a case, it is desirable by enlarging the elastic modulus of the jointing material 5 to reduce the stress generated in an insulator layer 3, to go away insulator layer 3, and to inhibit hiatus generating. Usually, the elastic modulus of the insulator layer 3 used is about 2.5 GPas, and when using this insulator layer 3, it sets the elastic modulus of the jointing material 5 as 10 or more GPas. By using material with a big elastic modulus for the jointing mat rial 5, the d formation at th time of the temperature change of an insulator lay r 3 can be restrained, and it becomes possible to go away insulator

layer 3 and to inhibit hiatus generating.

[0068] The [7th example] Drawing 15 is a plan in the state wher the cl sure resin, jointing material, and insulator layer of a semiconductor device by the 7th example of this invention were removed, and drawing 16 is the cross section of the semiconductor device shown in drawing 15 .

[0069] In drawing, conductive wiring and the insulator layer 3 are formed in semiconductor device root face 15a of the insulating tape 15, and conductive wiring consists of front wiring 2, bonding pad 2a, and land 2d. Opening 3a to which bonding pad 2a is exposed is prepared in the insulator layer 3. The rectangular semiconductor device 1 has fixed by the jointing material 5 to semiconductor device root face 15a of the insulating tape 15. A semiconductor device 1 and conductive wiring are electrically connected by the metal thin line 6, and the metal thin line 6 is joined to bonding pad 2a located outside the field of a semiconductor device 1. In a bonding pad 2a portion, opening 3a is prepared in the insulator layer 3, and the metal thin line 6 can be joined now. Front wiring 2 is formed so that the visible outline of a semiconductor device 1 may be intersected to land 2d arranged in the field of a semiconductor device 1 from bonding pad 2a and edge 1a may be crossed. In the portion in which land 2d is prepared, opening 16 is formed in the insulating tape 15, and the external terminal 8 is joined by land 2d inside opening 16. The external terminal 8 is formed in external terminal plane-of-composition 15b of an opposite side, and when it mounts a semiconductor device, it is joined to semiconductor device root face 15a of the insulating tape 15 by the position of a mounting substrate. Semiconductor device root face 15a of a semiconductor device 1, the metal thin line 6, and an insulating tape is covered with the closure resin 7.

[0070] The broad section 13 is formed in the front wiring 2 arranged among the front wiring 2 which crosses semiconductor device edge 1a at center-section part 1b of semiconductor device 1 each side. The broad section 13 of the front wiring 2 shown in drawing 15 is formed by making large wiring width of face between land 2d from a semiconductor device edge 1a portion.

[0071] A copper (Cu) foil or the copper foil which plated gold (Au), nickel (nickel), etc. on the front face is used for conductive wiring of front wiring 2 etc. The insulating tape 15 consists of material, such as a polyimide, and glass/epoxy. Material, such as gold (Au), silver (Ag), or aluminum (aluminum), is used for the metal thin line 6. The material which makes an epoxy resin a base material is used for the jointing material 5. The epoxy resin filled up for example, with the silica particle is used for the closure resin 7. In case a s miconductor device is mount d, the solder (for example, Pb-Sn

system eutectic solder) used widely is used for the ext rnal terminal 8.

[0072] According to th semiconductor devic of this example, deformation of th insulator layer at the time of a temperature change being added can be restrained by the front wiring which prepared the broad section, and generating and growth of the crack of an insulator layer can be inhibited.

[0073] The broad section 13 should just be formed in the front wiring 2 arranged like drawing 15 at least at center-section part 1b of each side of a semiconductor device 1. In the semiconductor device which carried the rectangular semiconductor device 1 like this example, center-section part 1b of semiconductor device each side will be in plane strain condition, and the stress generated in the direct lower part of semiconductor device edge 1a becomes large. Therefore, since the probability generated in this position becomes large, an open circuit of front wiring 2 can prevent an open circuit of front wiring by restraining the variation rate of the insulator layer 3 in this portion.

[0074] The example shown in drawing 15 shows the example which uses the metal thin line 6 for the electrical installation of a semiconductor device 1 and conductive wiring. Connection using the detailed bump by the foil-like lead and flip chip assembly technique which may make both connection by methods other than a metal thin line, for example, are used with TAB technology is made.

[0075] Moreover, the example shown in drawing 15 showed the example which forms the broad section 13 in the front wiring 2 between land 2d from a semiconductor device edge 1a portion. Since the deformation of an insulator layer 3 serves as the maximum by the minimum and edge 1a at the center of a semiconductor device 1, it goes away insulator layer 3 and hiatus are generated in a semiconductor device edge 1a portion. For this reason, an indispensable effect can be acquired if deformation of an insulator layer 3 is restrained in a semiconductor device edge 1a portion. Therefore, the broad section 13 should just be formed in a part for the direct lower part of semiconductor device edge 1a at least, as shown in the plan of drawing 17. In addition, drawing 18 is the cross section of the semiconductor device shown in drawing 17 . In the case of the semiconductor device which cannot enlarge wiring capacity, an example like drawing 17 becomes effective from the demand of high-speed operation especially.

[0076] [Octavus example] It is the cross section of the semiconductor device with which it is a plan in the state where the semiconductor device, the closure resin, and the insulator layer were removed, and drawing 20 showed th s miconductor device according [drawing 19] to the octavus example of this inv ntion to drawing 19 .

[0077] Since the basic composition as a semiconductor device is common in the 7th example, it omits explanation. At this exampl , by the front wiring group 14 by which two or more front wiring 2 are arranged among front wiring 2 at abbreviation parallel, the broad section 13 is formed in the front wiring located in edge 14a of a front wiring group, and wiring width of face is large from the front wiring located in internal 14b of a front wiring group. The broad section 13 of the front wiring shown in drawing 19 is formed by making large wiring width of face between land 2d from a semiconductor device edge 1a portion.

[0078] According to the semiconductor device shown in this example, by forming the broad section in the front wiring of the aforementioned front wiring group located in an edge at least, pinning can be carried out and generating and growth of the crack of an insulator layer can be inhibited with the conductive wiring which prepared the broad section of both ends for deformation of the insulator layer at the time of a temperature change being added.

[0079] The example shown in drawing 19 showed the example which forms the broad section 13 by land 2d from the semiconductor device edge 1a portion of the front wiring 2 located in both-ends 14a of the front wiring group 14. Since the deformation of an insulator layer 3 serves as the maximum by semiconductor device edge 1a, it goes away insulator layer 3 and hiatus are generated in an edge 1a portion. For this reason, an indispensable effect will be acquired if deformation of an insulator layer is restrained in a semiconductor device edge 1a portion. Therefore, the broad section 13 should just be formed in a part for the direct lower part of semiconductor device edge 1a at least. Thus, it becomes effective to make the formation range of the broad section small when it is the semiconductor device which cannot enlarge wiring capacity from the demand of high-speed operation.

[0080] The [9th example] It is the cross section of the semiconductor device with which it is a plan in the state where the semiconductor device, the closure resin, and the insulator layer were removed, and drawing 22 showed the semiconductor device according [drawing 21] to the 9th example of this invention to drawing 21 .

[0081] Since the basic composition as a semiconductor device is common in the 7th example, it omits explanation. In this example, the wiring width of face of the front wiring 12 extended so that edge 1a of a semiconductor device may be crossed among front wiring 2 is larger than front wiring 2 other than this. As for the front wiring 12 which crosses semiconductor device edge 1a shown in drawing 21 , the width of face of all wiring between land 2d from bonding pad 2a is large.

[0082] According to the semiconductor device of this xample, deformation of the

insulator layer at the tim of a temperature change being added can be restrain d by the front wiring which prepared the broad section, and generating and growth of the crack of an insulator layer can be inhibited.

[0083] The example shown in drawing 21 showed the example which makes broader than front wiring other than this front wiring 12 which crosses semiconductor device edge 1a. Since the deformation of an insulator layer 3 serves as the maximum by the minimum and edge 1a at the center of a semiconductor device 1, it goes away insulator layer 3 and hiatus are generated in a semiconductor device edge 1a portion. For this reason, an indispensable effect can be acquired if deformation of an insulator layer 3 is restrained in a semiconductor device edge 1a portion. Therefore, the part which makes wiring width of face large should just be a part for the direct lower part of semiconductor device edge 1a at least.

[0084] The [10th example] It is the cross section of the semiconductor device with which it is a plan in the state where the semiconductor device, the closure resin, and the insulator layer were removed, and drawing 24 showed the semiconductor device according [drawing 23] to the 10th example of this invention to drawing 23 .

[0085] Since the basic composition as a semiconductor device is common in the 7th example, it omits explanation. center-section part 15c in the 1st page of the semiconductor device in which it is semiconductor device root face 15a of an insulating tape, and land 2d is not formed in this example -- a rectangular deformation restraint -- the member 17 is formed a deformation restraint -- as for a member 17, it is desirable to constitute from same material as front wiring 2, and it uses the material which made copper (Cu) etc. the shape of a foil By preparing the member of the tabular constituted from a copper rigid big material in the insulating tape front face within a semiconductor device side, the effect which restrains deformation of the insulator layer by the temperature change can be acquired.

[0086] According to the semiconductor device shown in this example, by the deformation restricted member, deformation of an insulator layer can be restrained and deformation can be made small. By this, generating and growth of the crack of an insulator layer can be suppressed.

[0087] the example shown in drawing 23 -- a deformation restraint -- the example which forms a member 17 in the same rectangle as the configuration of a semiconductor device 1 was shown In the semiconductor device which carried the rectangular semiconductor device 1 like this example, the amount of [of a semiconductor devic] ach side center section will be in plane strain condition, and the stress generated in the semiconductor device edge 1a direct lower part in this

portion becomes large. Therefore, an open circuit f front wiring can prevent an open circuit f front wiring, if the variation rat of th insulator lay r 3 in this portion is restrained at least, since the probability generated in this position becomes large. the cross-joint type deformation restraint which is in agreement with the center line which passes along two sides which a semiconductor device counters in order that drawing 25 may reduce the deformation of the insulator layer for the center section of semiconductor device each side -- it is the example in which the member 17 was formed a deformation restraint -- by making a member 17 into a configuration like drawing 25 , deformation of the insulator layer for the center section of semiconductor device each side can be restrained Moreover, by reducing the amount of the copper foil used, the amount of curvatures of an insulating tape can be reduced and the work which fixes a semiconductor device on an insulating tape can be done easy.

[0088] The [11th example] Drawing 26 is the cross section of the semiconductor device by the 11th example of this invention.

[0089] Since the basic composition as a semiconductor device is common in the 7th example, it omits explanation. At this example, since opening 3b is prepared in the insulator layer 3 at a part for the direct lower part of semiconductor device edge 1a, in this portion, an insulator layer 3 does not exist but the closure resin 7 intervenes between a semiconductor device 1 and the insulating tape 15. By making the big closure resin of toughness placed between parts for the direct lower part of semiconductor device edge 1a from the material used for an insulator layer 3, semiconductor device edge 1a can be left and generating of hiatus can be suppressed.

[0090] The [12th example] Drawing 27 is the cross section of the semiconductor device by the 12th example of this invention, and drawing 28 is a plan in the state where the semiconductor device, closure resin, and insulator layer of the semiconductor device shown in drawing 27 were removed.

[0091] Since the basic composition as a semiconductor device is common in the 7th example, it omits explanation. In this example, it is semiconductor device root face 15a of an insulating tape, and to center-section part 15c in the 1st page of the semiconductor device in which land 2d is not formed, opening 18 is formed in the insulator layer 3, and the jointing material 5 has covered semiconductor device root face 15a of an insulating tape by center-section part 15c. That is, the insulator layer 3 is formed in the portion in which front wiring 2 and land 2d are formed in portions oth r than bonding pad 2a, and the field out of the 1st page of a semiconductor

device.

[0092] Since the pulse duty factor of th insulator layer within a semiconductor device side decreases by not forming an insulator layer 3 in center-section part 15c within a semiconductor device side, the deformation of the whole insulator layer by the temperature change becomes small, and generating and growth of the crack of an insulator layer come to be suppressed.

[0093] In the semiconductor device shown in drawing 27 , opening 18 was formed in center-section part 15c, and the insulator layer 3 showed the example of a wrap for the front wiring 2 in the 1st page of a semiconductor device, and land 2d. In order that an insulator layer 3 may reduce further the volume occupied in a semiconductor device side, it does not interfere, even if it prepares opening between front wiring 2 and land 2d. By forming an insulator layer 3 so that front wiring 2 and the land 2d circumference may be covered at least, the deformation of an insulator layer can be reduced further.

[0094] The [13th example] Drawing 29 is the cross section of the semiconductor device by the 13th example of this invention. Since the basic composition as a semiconductor device is common in the 7th example, it omits explanation. With the semiconductor device of this example, equivalent [in an insulator layer 3 / to the elastic modulus of the jointing material 5] or it forms with the material which has an elastic modulus not more than it. Since deformation of the insulator layer itself becomes easy even when a crack occurs in an insulator layer 3 by forming an insulator layer 3 into low elasticity, the stress generated at the nose of cam of a crack can be eased by deformation. Therefore, the effect which suppresses growth of the crack by the repeat of a temperature change can be acquired, and an open circuit of conductive wiring can be prevented.

[0095] The material whose elastic modulus is usually about 1 GPa is used for the jointing material 5. Therefore, an elastic modulus chooses and uses the material of 1 or less GPa for an insulator layer 3.

[0096] Although it goes away insulator layer 3 and hiatus generating and growth can be inhibited by low elasticity-ization of an insulator layer 3 as described above, the elastic modulus of an insulator layer 3 may not be able to be made low from the restrictions at the time of forming conductive wiring and an insulator layer 3 in the insulating tape 15 etc. In such a case, it is desirable by enlarging the elastic modulus of the jointing material 5 to reduce the stress generated in an insulator layer 3, to go away insulator layer 3, and to inhibit hiatus generating. Usually, the elastic modulus of the insulator layer 3 us d is about 2.5 GPas, and wh n using this insulator layer 3,

it sets the elastic modulus of the jointing mat rial 5 as 10 or more GPas. By using material with a big elastic modulus for the jointing material 5, the deformation at the time of the temperature change of an insulator layer 3 can be restrained, and it becomes possible to go away insulator layer 3 and to inhibit hiatus generating.

[0097]

[Effect of the Invention] Since the stress which can make small deformation of the insulator layer at the time of a temperature change being added according to [like] this invention described above, and is generated in an insulator layer can be reduced, it becomes possible to prevent open-circuit generating of the conductive wiring inside a semiconductor device, and a reliable semiconductor device can be offered.

[Brief Description of the Drawings]

[Drawing 1] The plan in the state where the member of the printed-circuit board upper part of the semiconductor device by the 1st example of this invention was removed.

[Drawing 2] The cross section of the semiconductor device shown in drawing 1 .

[Drawing 3] The plan in the state where the member of the printed-circuit board upper part which shows other aspects of the 1st example shown in drawing 1 was removed.

[Drawing 4] The plan in the state where the member of the printed-circuit board upper part of the semiconductor device by the 2nd example of this invention was removed.

[Drawing 5] The cross section of the semiconductor device shown in drawing 4 .

[Drawing 6] The plan in the state where the member of the printed-circuit board upper part which shows other aspects of the 2nd example shown in drawing 4 was removed.

[Drawing 7] The plan in the state where the member of the printed-circuit board upper part of the semiconductor device by the 3rd example of this invention was removed.

[Drawing 8] The cross section of the semiconductor device shown in drawing 7 .

[Drawing 9] The plan in the state where the member of the printed-circuit board upper part which shows other aspects of the 3rd example shown in drawing 7 was removed.

[Drawing 10] The plan in the state where the member of the printed-circuit board upper part of the semiconductor device by the 4th example of this invention was removed.

[Drawing 11] The cross section of the semiconductor device shown in drawing 10 .

[Drawing 12] The plan in the state where the member of the printed-circuit board upper part of the semiconductor device by the 5th example of this invention was removed.

[Drawing 13] Th cross s ction of th semiconductor device shown in drawing 12 .

[Drawing 14] The cross s ction showing th s miconductor device by the 6th example of this invention.

[Drawing 15] The plan in the state wh re the memb r of the insulating tape upper part which shows the semiconductor device by th 7th example f this inv ntion was removed.

[Drawing 16] The cross section of the semiconductor device shown in drawing 15 .

[Drawing 17] The plan in the state where the member of the printed-circuit board upper part which shows other aspects of the 7th example shown in drawing 15 was removed.

[Drawing 18] The cross section of the semiconductor device shown in drawing 17 .

[Drawing 19] The plan in the state where the member of the insulating tape upper part of the semiconductor device by the octavus example of this invention was removed.

[Drawing 20] The cross section of the semiconductor device shown in drawing 19 .

[Drawing 21] The plan in the state where the member of the insulating tape upper part of the semiconductor device by the 9th example of this invention was removed.

[Drawing 22] The cross section of the semiconductor device shown in drawing 21 .

[Drawing 23] The plan in the state where the member of the insulating tape upper part of the semiconductor device by the 10th example of this invention was removed.

[Drawing 24] The cross section of the semiconductor device shown in drawing 23 .

[Drawing 25] The plan in the state where the member of the insulating tape upper part which shows other aspects of the 10th example shown in drawing 23 was removed.

[Drawing 26] The cross section showing the semiconductor device by the 11th example of this invention.

[Drawing 27] The cross section of the semiconductor device by the 12th example of this invention.

[Drawing 28] The plan in the state where the member of the insulating tape upper part of the semiconductor device shown in drawing 27 was removed.

[Drawing 29] The cross section of the semiconductor device by the 13th example of this invention.

[Drawing 30] The cross section showing the example of the conventional BGA type semiconductor device

[Drawing 31] The plan in the state where are the conventional semiconductor device shown in drawing 30 , and the member of the printed-circuit board upper part was removed.

[Drawing 32] The partial cross-section enlarged view explaining the state of the crack of an insulator layer.

[Drawing 33] Drawing showing the result which analyzed the relation betw en conductive wiring width of face and generating stress with the finite element method.

[Drawing 34] Drawing showing the result which analyzed the elastic modulus of an insulator layer, and the relation of gen rating stress with th finite lement method.

[Drawing 35] Drawing showing the result which analyzed the elastic modulus of jointing material, and the relation of the generating stress on the front face of an insulator layer with the finite element method.

[Description of Notations]

1 [-- Front wiring, 2a / -- Bonding pad,] -- A semiconductor device, 1a -- A semiconductor device edge, 2 2b [-- A land, 3 / -- Insulator layer,] -- A through hole, 2d -- Internal wiring, 2d 4 -- A printed-circuit board, 4a -- The semiconductor device root face of a printed-circuit board, 5 [-- A closure resin, 8 / -- An external terminal, 9 / -- Insulator layer,] -- Jointing material, 6 -- A metal thin line, 7 10 [-- The front wiring, 13 which cross a semiconductor device edge / -- The broad section, 14 / -- A front wiring group, 15 / -- An insulating tape, 15a / -- The semiconductor device root face of an insulating tape, 16 / -- Opening of an insulating tape 17 / -- A deformation restricted member, 18 / -- Opening of an insulator layer] -- The crack of an insulator layer, 11 -- The crack of jointing material, 12